REMARKS/ARGUMENTS

In the Office Action mailed July 11, 2008, claims 1-7 were rejected. In response, claim 1 has been amended. Additionally, claim 2 has been canceled and claims 9-20 have been added. Applicants hereby request reconsideration of the application in view of the amended claim, the added claims, and the below-provided remarks.

Claim Rejections under 35 U.S.C. 112

Claims 1-7 were rejected under 35 U.S.C. 112 as allegedly "being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." However, Applicants respectfully submit that these claims are acceptable for the reasons provided below.

Claim 1 has been amended to include all the limitations of claim 2. Claim 2 has been canceled. With regard to amended claim 1, the Office Action states that "the plurality of outputs are not interrelated to any other elements among the claim." Amended claim 1 recites "a functional block being coupled between the plurality of inputs and the plurality of outputs only in a functional mode of the integrated circuit" and "a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit." Therefore, Applicants respectfully submit that the plurality of outputs is interrelated to other elements among the claim. With regard to amended claim 1, the Office Action also states that "it is not clear how the function block and the logic gates are interrelated to each others." Applicants respectfully submit that it is not required that these two elements are interrelated. With regard to claims 3-7, Applicants respectfully submit that claims 3-7 are acceptable based on an acceptable amended claim 1.

Claim Rejections under 35 U.S.C. 103

Claims 1-7 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Itaya (U.S. Pat. No. 6,271,700). However, Applicants respectfully submit that these claims are patentable over Itaya for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to include all the limitations of claim 2. Additionally, claim 1 has been amended to particularly point out that a functional block is coupled between a plurality of inputs and a plurality of outputs of an integrated circuit only in a functional mode of the integrated circuit and to recite "*a programmable switch configured to switch between the functional mode and the test mode of the integrated circuit, wherein the programmable switch is coupled between an input from the plurality of inputs, the functional block and the first input of each logic gate from the plurality of logic gates.*" Support for the addition of the programmable switch can be found in Applicants' specification at, for example, FIG. I reference number 162 and page 5 lines 21-30. As amended, claim 1 recites

> "An integrated circuit, comprising:
> a plurality of inputs;
> a plurality of outputs;
> a functional block being coupled between the plurality of inputs and the plurality of outputs only in a functional mode of the integrated circuit;
> a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit, the test arrangement comprising a plurality of logic gates, each logic gate from the plurality of logic gates having a first input coupled to an input from the plurality of inputs; and
> a programmable switch configured to switch between the functional mode and the test mode of the integrated circuit, wherein the programmable switch is coupled between an input from the plurality of inputs, the functional block and the first input of each logic gate from the plurality of logic gates,
> characterized by each logic gate from the plurality of gates having a further input coupled to a fixed logic value source." (emphasis added).

Applicants respectfully assert that Itaya fails to teach that a functional block is coupled between a plurality of inputs and a plurality of outputs "*only in a functional mode of the integrated circuit*" as recited in claim 1. Itaya teaches that a combinational circuit (11) is coupled to the inputs and outputs of a semiconductor integrated circuit (10A) in a normal operating mode and a scan mode, see FIG.1 and column 3, lines 35-44, and column 3, lines 47-64. Because Itaya fails to teach that the combinational circuit (11) is coupled to the inputs and outputs of the semiconductor integrated circuit (10A) only in one of the normal operating mode and the scan mode, Applicants respectfully assert that Itaya fails to teach that a functional block is coupled between a plurality of inputs and a plurality of outputs "*only in a functional mode of the integrated circuit*" as recited in claim 1. Therefore, Applicants respectfully assert that Itaya does not teach all

the limitations of amended claim 1. Accordingly, Applicants respectfully assert that a *prima facie* case of obviousness has not been established with respect to claim 1.

Dependent Claims 3-7

Claims 3-7 depend from and incorporate all of the limitations of the independent claim 1. Applicants respectfully assert that claims 3-7 are allowable at least based on an allowable claim 1.

New Claims 8-20

Claims 8-20 have been added. Applicants respectfully submit that these new claims are patentable over Itaya for the reasons provided below.

Independent Claim 8

Claim 8 includes all the limitations of original claim 1 and claim 5 as previously presented. Additionally, claim 8 includes the limitation, "*each logic gate from the plurality of logic gates having a first function and a second function*" and that "*the logic gate performs the first function when the multiplexer is switched to the input from the plurality of inputs and the second function when the multiplexer is switched to the fixed logic value source of the logic gate.*" Support for claim 8 can be found in Applicants' specification at, for example, original claim 1, claim 5 as previously presented, and page 3, lines 3-8.

Applicants respectfully assert that Itaya fails to teach that "*the logic gate performs the first function when the multiplexer is switched to the input from the plurality of inputs*" as recited in claim 8. Itaya teaches that a multiplexer (22) is coupled to a scan-in signal (SIN) and a scan mode signal (*SM) and provides an output to an AND gate (32), see FIG. 1. However, Itaya teaches that the AND gate (32) is closed when the multiplexers (22) selects the scan-in signal (SIN), see column 3 line 47-64. Because the AND gate (32) is closed when the multiplexers (22) selects the scan-in signal (SIN), the AND gate (32) does not perform any function when the multiplexers (22) selects the scan-in signal (SIN).

Therefore, Applicants respectfully assert that Itaya does not teach all the limitations of amended claim 8. Accordingly, Applicants respectfully assert that amended claim 8 is patentable over Itaya.

Dependent Claims 9-13

Support for new claims 9-13 can be found in Applicants' specification at, for example, original claims 2 and 3, claim 4 as previously presented, and original claims 6 and 7. Claims 9-13 depend from and incorporate all of the limitations of the independent claim 8. Applicants respectfully assert that claims 9-13 are allowable at least based on an allowable claim 8.

Independent Claim 14

Claim 14 includes all the limitations of original claim 1. Additionally, claim 14 includes the limitation "*the fixed logic value source includes a plurality of subsources, each subsource being arranged to provide the further input of at least one logic gate from the plurality of logic gates with a fixed logic value.*" Support for the amendment can be found in Applicants' specification at, for example, original claim 1, FIG. 1 and page 5, lines 3-10.

Applicants respectfully assert that Itaya fails to teach that "*the fixed logic value source includes a plurality of subsources, each subsource being arranged to provide the further input of at least one logic gate from the plurality of logic gates with a fixed logic value*" as recited in claim 14. Itaya teaches that AND gates (32-35) are coupled to a scan mode signal (*SM), see FIG. 1. However, Itaya does not teach that the scan mode signal (*SM) provides multiple sources of fixed logic values to AND gates (32-35).

Therefore, Applicants respectfully assert that Itaya does not teach all the limitations of amended claim 14. Accordingly, Applicants respectfully assert that amended claim 14 is patentable over Itaya.

Dependent Claims 15-20

Support for new claims 15-20 can be found in Applicants' specification at, for example, original claims 2 and 3, claims 4 and 5 as previously presented, and original

claims 6 and 7. Claims 15-20 depend from and incorporate all of the limitations of the independent claim 14. Applicants respectfully assert that claims 15-20 are allowable at least based on an allowable claim 14.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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